

June 2, 2004  
Case No. ATD00007 (9640/126)  
Serial No.: 10/612,590  
Filed: July 1, 2003  
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**CLAIM AMENDMENTS**

Claims 1-22 are currently pending in the application.

Of the above claims, Claims 10-16 are withdrawn from the application.

Please amend claims 1 and 17 as indicated below.

Please cancel claim 4.

This listing of claims 1-22 will replace all prior versions and listings of claims in the application:

1. (Currently amended) An integrated device with a corrosion-resistant capped bond pad, comprising:

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at least one aluminum bond pad on a semiconductor substrate;  
a layer of electroless nickel disposed on the aluminum bond pad;  
a layer of electroless palladium disposed on the electroless nickel; and  
a layer of immersion gold disposed on the electroless palladium;

wherein the layer of electroless nickel is formed on the  
aluminum bond pad by a zinc displacement plating process.

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2. (Original) The integrated device of claim 1 wherein the integrated device is selected from the group consisting of an integrated circuit, an analog circuit, a digital circuit, a radio-frequency device, a semiconductor sensor, an integrated sensor, a pressure sensor, a microelectromechanical device, a microoptoelectromechanical device, a sensor assembly, an integrated circuit assembly, a wire-bonded assembly, and a combination thereof.

3. (Original) The integrated device of claim 1 wherein the semiconductor substrate comprises one of a silicon wafer or a silicon die.

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4. (Cancelled)

5 (Original) The integrated device of claim 1 wherein the layer of electroless nickel has a thickness between 0.5 microns and 7.5 microns.

6. (Original) The integrated device of claim 1 wherein the layer of electroless palladium has a thickness between 0.2 microns and 1.0 micron.

7. (Original) The integrated device of claim 1 wherein the layer of immersion gold has a thickness between 0.05 microns and 0.25 microns.

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8. (Original) The integrated device of claim 1 further comprising:  
a layer of electroless gold disposed on the immersion gold.
9. (Original) The integrated device of claim 8 wherein the layer of  
electroless gold has a thickness between 0.1 microns and 1.5 microns.
10. (Withdrawn) A method of forming a capped bond pad, comprising:  
providing a plurality of aluminum bond pads on a semiconductor  
substrate;  
zincating a surface of the aluminum bond pads;  
plating a layer of electroless nickel on the zincated surface of the  
aluminum bond pads, wherein the zincated surface is displaced with the layer of  
electroless nickel;  
plating a layer of electroless palladium on the electroless nickel; and  
plating a layer of immersion gold on the electroless palladium.
11. (Withdrawn) The method of claim 10 wherein the provided  
semiconductor substrate comprises one of a silicon wafer or a silicon die.
12. (Withdrawn) The method of claim 10 wherein the layer of electroless  
nickel is plated to a thickness between 0.5 microns and 7.5 microns.

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13 (Withdrawn) The method claim 10 wherein the layer of electroless palladium is plated to a thickness between 0.2 microns and 1.0 micron.

14. (Withdrawn) The method of claim 10 wherein the layer of immersion gold is plated to a thickness between 0.05 microns and 0.25 microns.

15. (Withdrawn) The method of claim 10 further comprising:  
plating a layer of electroless gold on the immersion gold.

16. (Withdrawn) The method of claim 15 wherein the layer of electroless gold is plated to a thickness between 0.1 microns and 1.5 microns.

17. (Currently Amended) A semiconductor wafer with a plurality of capped bond pads, comprising:

a plurality of aluminum bond pads on a surface of the semiconductor wafer,

a layer of electroless nickel disposed on the aluminum bond pads;

a layer of electroless palladium disposed on the electroless nickel; and

a layer of immersion gold disposed on the electroless palladium,

wherein the layer of electroless nickel is formed on the aluminum bond [[pad]] pads by a zinc displacement plating process.

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18. (Original) The semiconductor wafer of claim 17, wherein the semiconductor wafer comprises a silicon substrate.

19. (Original) The semiconductor wafer of claim 17, wherein the semiconductor wafer comprises an integrated device selected from the group consisting of an integrated circuit, an analog circuit, a digital circuit, a radio-frequency device, a semiconductor sensor, an integrated sensor, a pressure sensor, a microelectromechanical device, a microoptoelectromechanical device, a wire-bondable device, and a combination thereof.

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20. (Original) The semiconductor wafer of claim 17, further comprising:  
a layer of electroless gold disposed on the immersion gold.

21. (Original) A capped bond pad for a corrosion-resistant integrated device, comprising:  
a layer of electroless nickel disposed on at least one aluminum bond pad;  
a layer of electroless palladium disposed on the electroless nickel; and  
a layer of immersion gold disposed on the electroless palladium,  
wherein the layer of electroless nickel is formed on the aluminum bond pad by a zinc displacement plating process.

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22. (Original) The capped bond pad of claim 21 further comprising:  
a layer of electroless gold disposed on the immersion gold
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